CURRICULUM VITAE

SANJAY KUMAR

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INDIA

Objective:

To pursue a dynamic and challenging career in an established firm that will offer me the best opportunity for further development and utilization of my abilities, skills and knowledge.

Educational Qualifications:

Examination	Discipline/ Specialization	Board/ University	Year of Passing	Grade/ Percentage
Ph.D.	Microelectronics	IIT (BHU), Varanasi	2018	**8.80**
M.Tech	Microelectronics	IIT (BHU), Varanasi	2013	**8.73**
B.Tech	Elecronics & Communication	Dr. B. C. Roy Engg. College, Durgapur	2010	**7.66**
Intermediate	PCM Group	S. K. M College, Nawada	2003	**73.80%**
Matriculation	All Subject	Gandhi Inter School, Nawada	2000	**68.50%**

Ph.D.

- **<u>Research Topic:</u> "Analytical Modeling and Simulation of Some Gate Structure Engineered Homo/Heterojunction Double-Gate Tunnel FETs"**

Under the supervision of Prof. Satyabrata Jit

Description: Tunnel field effect transistors (TFETs) has an unique property such as low subthrehold swing (SS), high ON-OFF current ratio, and reduced short channel effects (SCEs) which makes a suitable candidate for obtaining low power application. However, due to band-band tunnelling (BTBT) phenomenon, TFETs suffer from low ON current problem i.e. it does not full-fill requirement for international technology roadmap for semiconductor (ITRS). To overcome this problem, we have proposed some techniques using modeling and simulation to improve ON-state current such as low band gap materials, gate work function engineering, gate-oxide engineering, and heterojunction. The model results have been compared with the simulation data obtained using the commercially available ATLAS 2-D device simulator from SILVACO for the validity of the proposed model.

M.Tech:

- **<u>Research Topic</u>: "Analytical Modeling and ATLAS Based Simulation of Double-Gate (DG) MOSFETs with Gaussian-doping Profile"**

Under the supervision of Prof. Satyabrata Jit

Description: A 2-D analytical model for electrical characteristics such as surface potential, threshold voltage, subthreshold current and subthreshold swing (SS) of double-gate (DG) MOSFETs with vertical gaussian-like doping profile has been demonstrated in the dissertation. Parabolic approximation method has been used to derive the surface potential of DG MOSFETs. Accuracy of the proposed models is verified using the commercially available ATLAS^{TM}, a 2-D device simulator from SILVACO.

B.Tech:

- **<u>Project topic</u>: "Temperature Indicator and Controller using Microcontroller"**.

It is a temperature indicator cum controller that can be interfaced with a heater's coil to maintain the ambient temperature; the controller is based on AT89C51 microcontroller.

Work Experience:

- **Working as an Assistant Professor** in the Department of Electronics & Communication Engineering at IIIT Bhagalpur since 07 August 2018 till date.
- **Working as Teaching Assistant** under Prof. Satyabrata Jit for Analog Communication Systems during the even semester, session 2016-2017.
- **Worked as Teaching Assistant** under Prof. Satyabrata Jit for Signals and Systems during the odd semester, session 2016-2017.

- **Worked as Teaching Assistant** under Prof. Satyabrata Jit for Signals and Systems and Analog Communication Systems during session 2015-2016.

Area of Research Interests:

- Modeling of Conventional/Non-Conventional Semiconductor Devices and its RF/Analog application
- Characterization of Semiconductor Devices for Optoelectronics and Microelectronics using TCAD simulator.

Subjects of Interests:

- Basic Electronics
- Basic Electrical Engineering
- Solid State Devices
- Analog Circuits
- Digital Electronics
- LSI/VLSI Deign
- Microelectronics

Software Skills:

- Computation and Programming Software- MATLAB
- Simulation Software- ATLAS
- Operating Systems- Windows XP/ VISTA/7/8

Training & Workshops:

- Participated Short term Course on **"Modeling and Simulation of Advanced Semiconductor Devices"**, held at **IIT (BHU), Varanasi** during July 17th to 22th, 2017.
- Attended the Short Course on **"Modeling, Simulation and Characterization of Nano-Transistors"** organized by Department of Electrical engineering, **IIT Kanpur** during October 26th to 30th, 2015.
- Attended **"National Symposium on Research Methodology for Future researchers" (RMFR-2015)** conducted by **IIT (BHU), Varanasi.**
- Participated in one day Workshop on **"National e-Governance Plan"**, organized by Computer Centre, **IIT (BHU), Varanasi**.
- Attended workshop on **Digital Design in VLSI & Verilog HDL** conducted by **NVIDIA Graphics Pvt. Ltd., Bangalore** at IT-BHU, Varanasi.

Extra-Curricular Activities:

- Worked as **Coordinator** for celebration of Republic Day in IIIT Bhagalpur, 2018-2019.
- Worked as **Faculty-in-charge** in IIIT Bhagalpur, 2018-2019.
- Worked as **Mess Manager** in Vivekanand Hostel, IIT (BHU), Varanasi, 2014-2015.
- Participated in **The Institute Day** held at **IIT (BHU), Varanasi** during April 02-03, 2016.
- Participated in **The Institute Day** held at **IIT (BHU), Varanasi** during February 26-27, 2015.
- Participated in **four days Yoga Camp,** organized by **Banaras Hindu University Student's Council** during 28 Jan.- 28 Feb. 2012.

Personal Traits:

Dedicated towards responsibilities, Self-confident, Punctual, and Disciplined.

Personal Details:

Father's Name	**:**	Shri Ashok Singh
Mother's Name	**:**	Smt. Sheela Devi
Nationality	**:**	Indian
Gender	**:**	Male
Date of Birth	**:**	21/12/1984
Languages	**:**	English & Hindi
Present Address	**:**	Room No- 101, Department of Electronics and Communication Engg., IIIT Bhagalpur, Bhagalpur. Pin- 813210, India.
Permanent Address	**:**	S/o Ashok Singh, Saryug Prasad, Gola Road, Nawada (Bihar) Pin-805110, India.
Hobbies/Interests	**:**	Playing Badminton, Plantation

DECLARATION:

I, hereby, declare that all the information provided is true to the best of my knowledge and belief.

Sanjay Kumar

Date: 31/10/2019 **(Sanjay Kumar)**

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List of Publications

Published Papers in International Journals

1. **Sanjay Kumar**, Ekta Goel, Kunal Singh, Balraj Singh, Prince Kumar Singh, Kamlaksha Baral and Satyabrata Jit, "2-D Analytical Modelinng of the Electrical Characteristics of Dual-Material DG TFETs with a SiO2/High-k Stacked Gate-Oxide Structure", ***IEEE Transactions on Electron Devices,*** Vol 64, pp. 960-968, (2017). (Impact Factor: 2.605)
2. **Sanjay Kumar**, Ekta Goel, Kunal Singh, Balraj Singh, Mirgender Kumar and Satyabrata Jit, "A Compact 2D Analytical Model for Electrical Characteristics of Double-Gate Tunnel Field-Effect Transistors with a SiO2/High-k Stacked Gate-Oxide Structure", ***IEEE Transactions on Electron Devices,*** Vol 63, pp. 3291-3299, (2016). (Impact Factor: 2.605)
3. **Sanjay Kumar**, Kunal Singh, Sweta Chander Ekta Goel, Balraj Singh, Prince Kumar Singh, Kamlaksha Baral and Satyabrata Jit, "2-D Analytical Drain Current Model of Heterojunction DG TFETs with a SiO2/High-k Stacked Gate-Oxide Structure", ***IEEE Transactions on Electron Devices*** Vol 65, no.1 pp. 331-338, Jan.(2018). (Impact Factor: 2.605)
4. **Sanjay Kumar**, Kunal Singh, Sweta Chander Ekta Goel, Balraj Singh, Prince Kumar Singh, Kamlaksha Baral and Satyabrata Jit, "2-D Analytical Modelinng for Electrical Characteristics of Dual-Material Heterogenious Gate DG TFETs with Localized Interface Charges", ***IEEE Transactions on Electron Devices.***(Under Review)
5. Ekta Goel, **Sanjay Kumar**, Kunal Singh, Balraj Singh, Mirgender Kumar, and Satyabrata Jit, "2-D Analytical Modeling of Threshold Voltage for Graded-Channel Dual-Material Double-Gate MOSFETs", ***IEEE Transactions on Electron Devices,*** Vol 63, pp. 966-973, (2016). (Impact Factor: 2.605)
6. Mirgender Kumar, **Sanjay Kumar**, Ekta Goel, Kunal Singh, Balraj Singh, and Satyabrata Jit, "Strain-Induced Plasma Radiation at Terahertz Domain in Strained-Si-on-Insulator MOSFETs*", **IEEE Transactions on Plasma Science***, Vol. 44, no. 3, pp. 245-249. (Impact Factor: 1.052)
7. Balraj Singh, Deepti Gola, Kunal Singh, Ekta Goel, **Sanjay Kumar**, and Satyabrata Jit, "*Two-Dimensional Analytical Threshold Voltage Model for Dielectric Pocket Double-Gate Junctionless FETs by Considering Source/Drain Depletion Effect*", ***IEEE Transactions on Electron Devices,*** Vol 64, pp. 901-907, (2017). (Impact Factor: 2.605)
8. Balraj Singh, Deepti Gola, Kunal Singh, Ekta Goel, **Sanjay Kumar** and Satyabrata Jit, "Analytical Modeling of Channel Potential and Threshold Voltage of Double Gate Junctionless Field Effect Transistors with a Vertical Gaussian-Like Doping Profile", ***IEEE Transactions on Electron Devices***, Vol 63, pp. 2299-2305, (2016). (Impact Factor: 2.605)
9. Ekta Goel, **Sanjay Kumar**, Kunal Singh, Balraj Singh and Satyabrata Jit, "Two-dimensional model for subthreshold current and subthreshold swing of graded-channel dual-material doublegate (GCDMDG) MOSFETs", ***Superlattices and Microstructures,*** Vol 106, pp. 147-155, (2017). (Impact Factor: 2.207)
10. Kunal Singh, **Sanjay Kumar**, Ekta Goel, Balraj Singh, Mirgender Kumar, Sarvesh Dubey and Satyabrata Jit, "Subthreshold Current and Swing Modeling of Gate Underlap DG MOSFETs with Source/Drain Lateral Gaussian Doping Profile", ***Journal of Electronic***

Materials (Accepted).(Impact Factor: 1.491)

11. Kunal Singh, **Sanjay Kumar**, Ekta Goel, Balraj Singh, Mirgender Kumar, Sarvesh Dubey and Satyabrata Jit, "Effects of source/drain elevation and side spacer dielectric on drivability performance of non-abrupt ultra shallow junction gate underlap GAA MOSFETs", ***Indian Journal of Physics***, (Accepted).(Impact Factor: 1.166)
12. Kunal Singh, **Sanjay Kumar**, Ekta Goel, Balraj Singh, Prince Kumar Singh, K. Baral, Hemant Kumar, and S. Jit, "Effects of Elevated Source/Drain and Side SpacerDielectric on the Drivability Optimization of Non-abrupt Ultra Shallow Junction Gate Underlap DG MOSFETs", ***Journal of Electronic Materials*** June 2017. (Impact Factor: 1. 491)
13. Kunal Singh, **Sanjay Kumar**, Pramod Kr Tiwari, A. B. Yadav, Sarvesh Dubey and Satyabrata Jit, "Semianalytical Threshold Voltage Model of a Double-Gate Nanoscale RingFET for Terahertz Applications in Radiation-Hardened (Rad-Hard) Environments", ***Journal of Electronic Materials,*** Vol. 48, pp. 6366-6371, Oct. 2019.
14. Sweta Chander, Sanjeet Kumar Sinha, **Sanjay Kumar**, P. K. Singh, Kamlaksha Baral, Kunal Singh, and Satyabrata Jit, "Temperature Analysis of Ge/Si Heterojunction SOI-Tunnel FET", ***Superlattices and Microstructures,*** Vol 110, pp. 162-170, 2017.(Impact Factor: 2.20)
15. P. K. Singh, Kamlaksha Baral, **Sanjay Kumar**, Sweta Chander and Satyabrata Jit, "Analytical Drain Current Model of Stacked Oxide SiO2/HfO2 Cylindrical Gate Tunnel FETs with Oxide Interface Charge", ***Indian Journal of Physics***, pp. 1-9, June 2019.
16. Sweta Chander, Srimanta Baishya, **Sanjay Kumar**, P. K. Singh, Kamlaksha Baral, and Satyabrata Jit, "Two-Dimensional Analytical Modeling for Electrical Characteristics of Ge/Si SOI-Tunnel FinFETs", ***Superlattices and Microstructures,*** Vol. 131, pp. 30-39, July 2019.
17. Ekta Goel, Balraj Singh, **Sanjay Kumar**, Kunal Singh, and Satyabrata Jit, "Analytical threshold voltage modelling of ion-implanted strained-Si doublematerialdouble-gate (DMDG) MOSFETs", ***Indian Journal of Physics***, Vol 91, pp. 383-390, 2017. (Impact Factor: 1.166)
18. Ekta Goel, Balraj Singh, Kunal Singh, **Sanjay Kumar**, and Satyabrata Jit, "2-D analytical modeling of subthreshold current and subthreshold swing for ion-implanted strained-Si double-material double-gate (DMDG) MOSFETs", ***Indian Journal of Physics***, Vol 91, pp. 1069-1076, September, 2017. (Accepted). (Impact Factor: 1.166)
19. Balraj Singh, Deepti Gola, Ekta Goel, **Sanjay Kumar**, Kunal Singh, and Satyabrata Jit, "Dielectric Pocket Double Gate Junctionless FET: A New MOS Structure with Improved Subthreshold Characteristics for Low Power VLSI Applications", ***Journal of Computational Electronics,*** Vol 15, pp. 502-507, (2016). (Impact Factor: 1.104)
20. Kunal Singh, Mirgender Kumar, Ekta Goel, Balraj Singh, Sarvesh Dubey, **Sanjay Kumar**, and Satyabrata Jit, "Analytical Modeling of Potential Distribution and Threshold Voltage of Gate Underlap DG MOSFETs with a Source/Drain Lateral Gaussian Doping Profile", ***Journal of Electronic Materials,*** Vol 45, pp. 2184-2192, (2016**)**. (Impact Factor: 1.491)
21. Balraj Singh, Trailokya Nath Rai, Deepti Gola, Kunal Singh, Ekta Goel, **Sanjay Kumar**, Pramod Kumar Tiwari and Satyabrata Jit, "Ferro-electric stacked gate oxide heterojunction electro-statically doped source/drain double-gate tunnel field effect transistors: A superior structure", ***Materials Science in Semiconductor Processing,*** Vol 71, pp. 161-165, (2017). (Impact Factor: 2.207)
22. Balraj Singh, Deepti Gola, Kunal Singh, Ekta Goel, **Sanjay Kumar**, and Satyabrata Jit, "Analytical modeling of subthreshold characteristics of ion-implanted symmetric double

gate junctionless field effect transistors", ***Materials Science in Semiconductor Processing,*** Vol 58, pp. 82-88, (2017). (Impact Factor: 2.207)

23. H. Kumar, Y. Kumar, K. Singh, **S. Kumar**, G. Rawat, C. Kumar, B.N. Pal and S. Jit "Kink effect in TiO2 embedded ZnO quantum dot-based thin film transistors", ***Electronics Letter,*** Vol. 53, no. 4, pp. 262-264, Feb. 2017. (Impact Factor: 0.9)
24. Gopal Rawat, **Sanjay Kumar**, Ekta Goel, Mirgender Kumar, Sarvesh Dubey and S. Jit, "Analytical Modeling of Subthreshold Current and Subthreshold Swing of Gaussian-Doped (GD) Strained-Si-on-Insulator (SSOI) MOSFETs", ***Journal of Semiconductors*** .,Vol. 35, no. 8, pp. 084001-8, Aug. 2014.
25. Gopal Rawat, Ekta Goel, **Sanjay Kumar**, Mirgender Kumar, Sarvesh Dubey and S. Jit, "Analytical Modeling of Threshold Voltage of Ion-Implanted Strained-Si-on-Insulator (SSOI) MOSFETs", ***Journal of Nanoelectronics and Optoelectronics***, Vol. 9, no. 3, pp. 442-448, June 2014. (Impact Factor: 0.675)

List of International Conference (Oral/Poster) Presentations:

1. **Sanjay Kumar**, Kunal Singh, Sweta Chander, Prince Kumar Singh, Kamalaksha Baral, and S. Jit, "Influence of localized Interface Charges on Drain Current of Dual-Material Double-Gate Tunnel FETs", *International Conferences for Convergence of Technology **(I2CT)**, 7-8th April*, Pune2018.
2. **Sanjay Kumar**, Kamalaksha Baral, Sweta Chander, Prince Kumar Singh, Balraj Singh and S. Jit, "Performance Evaluation of Double Gate III-V Heterojunction Tunnel FETs with SiO2/HfO2 Gate Oxide Structure", *IEEE International Symposium on Devices, Circuits and Systems **(ISDCS),*** 29th - 31st March IIST Shivpur, India 2018.
3. **Sanjay Kumar**, P. K. Singh, Sweta Chander, Ashvini Rahangdale , K. Baral, and S. Jit, "Dual-Material Ferroelectric Stacked Gate SiO2/PZT SOI Tunnel FETs with Improved Performance: Design and Analysis, 5*th International Conference on Signal Processing and Integrated Networks **(SPIN))***, @Amity university, Noida, 2018.
4. **Sanjay Kumar**, Kunal Singh, Sweta Chander, Prince Kumar Singh, Kamalaksha Baral, and S. Jit, "Temperature Sensitivity Analysis of Double Gate Tunnel FETs with SiO2/HfO2 Stacked Gate Oxide Structure", *Nanotechnology for Instrumentation & measurement Workshop, **NANOfIM*** ,India 2017.
5. **Sanjay Kumar**, Ashvini Rahangdale, Sweta Chander, Prince Kumar Singh, Kamalaksha Baral, and S. Jit, "A Simulation Based Study for Electrical Characteristics of SOI TFETs With Ferroelectric Stacked Gate Oxide Structure", *14th IEEE India Council International Conference **(INDICON),*** IIT Roorkee ,India, 2017.
6. **Sanjay Kumar**, Ekta Goel, Kunal Singh, Balraj Singh, Mirgender Kumar, and S. Jit, "A 2D Analytical Model of Double-Gate (DG) Tunnel-Field-Effect Transistor (TFET): Impact of Shortest Tunneling Distance", *18th International Workshop on the Physics of Semiconductor Devices **(IWPSD)***, @Indian Institute of Science, Banglore, 2015.
7. **Sanjay Kumar**, Ekta Goel, Kunal Singh, Mirgender Kumar and S. Jit, "Surface Potential Based Subthreshold Current Modeling of DG MOSFETs with Non-uniform Doping in the Vertical Direction", *4th International Conference on Current Developments in Atomic,*

Molecular & Optical Physics with Applications ***(CDAMOP-2015)***, 11th-14th March, 2015 held at University of Delhi, Delhi.

8. Prince Kumar Singh, **Sanjay Kumar**, Sweta Chander, Kamalaksha Baral, and S. Jit, "Impact of Strain on Electrical Characteristic of Double-Gate TFETs with a SiO2/HfO2 Stacked Gate-Oxide Structure", *14th IEEE India Council International Conference* ***(INDICON),*** IIT Roorkee ,India, 2017.
9. Kamalaksha Baral, Prince Kumar Singh, **Sanjay Kumar**, Sweta Chander, and S. Jit, "Performance Analysis and Optimization of Nanotube Junctionless Accumulation MOSFETs with Lateral HfO2/SiO2 Gate-oxide Structure", *Nanotechnology for Instrumentation & measurement Workshop,* ***NANOfIM*** ,India 2017.
10. Balraj Singh, Deepti Gola, , Kunal Singh, Ekta Goel, **Sanjay Kumar** and Satyabrata Jit, "Temperature Sensitivity Analysis of DG Junctionless FETs with Vertical Gaussian Doping Profile" *IEEE International Conference on Micro-Electronics and Telecommunication Engineering*, 2016, India.
11. Balraj Singh, Deepti Gola, **Sanjay Kumar** , Kunal Singh, Ekta Goel, and Satyabrata Jit, "Performance Evaluation of Double Gate Junctionless Field Effect Transistor with Vertical Gaussian Doping Profile" *IEEE International Conference On Recent Trends In Electronics Information Communication Technology*, May 20-21, 2016, India.
12. Ekta Goel**,** Kunal Singh, **Sanjay Kumar**, Balraj Singh, M. Kumar and S. Jit, "Impact of Heterogeneous Gate Dielectric on Strained Silicon Double-Gate Tunnel Field Effect Transistor", *18th International Workshop on the Physics of Semiconductor Devices* ***(IWPSD)***, @Indian Institute of Science, Banglore, 2015.
13. Ekta Goel, **Sanjay Kumar**, Mirgender Kumar and S. Jit, "Two Dimensional Analytical Threshold Voltage Model of Strained Silicon Double-Gate (DG) MOSFETs with vertical Gaussian-like Doping Profile", *4th International Conference on Current Developments in Atomic, Molecular & Optical Physics with Applications* ***(CDAMOP-2015)***, 11th-14th March, 2015 held at University of Delhi, Delhi.
14. Varun Goel, Sanjay Sharma, **Sanjay Kumar**, and S. Jit "Two Dimensional Analytical Model for Threshold Voltage of Graded-Channel SOI MOSFETs" *2nd IEEE International Conference on Emerging Electronics (ICEE-2015)*during 3th-6th December, 2014 held at IISC Bangalore.
15. **Sanjay Kumar**, Ekta Goel, Gopal Rawat, Mirgender Kumar, S. Dubey, S. Jit, "Threshold Voltage Modeling of Short-Channel DG MOSFETs with Non-Uniform Doping in the Vertical Direction", *17th International Workshop on the Physics of Semiconductor Devices* ***(IWPSD)***, @Amity university, Noida, **Springer conference proceeding**, pp. 263-266, 2014.
16. Ekta Goel, **Sanjay Kumar**, Gopal Rawat, Mirgender Kumar, S. Dubey, S. Jit, "Two Dimensional Model for Threshold Voltage Roll-Off of Short Channel High-*k* Gate-Stack Double-Gate (DG) MOSFETs", *17th International Workshop on the Physics of Semiconductor Devices* ***(IWPSD)***, @Amity university, Noida, **Springer conference proceeding**, pp. 193-196, 2014.
17. **Sanjay Kumar**, Ekta Goel, Gopal Rawat, Kunal Singh, Mirgender Kumar, Sarvesh Dubey and S. Jit, "Surface Potential Based Subthreshold Swing Modeling of Symmetric Double-Gate (DG) MOSFETs with a Vertical Gaussian Doping Profile", *International Conference on Nanoscience & Nanotechnology* ***(ICNN-2013)***during 18-20 November, 2013 at Babasaheb Bhimrao Ambedkar University, Lucknow, U.P., India.
18. Ekta Goel, **Sanjay Kumar**, Gopal Rawat, Mirgender Kumar, Sarvesh Dubey and S. Jit, "An

Analytical Model for Threshold Voltage Roll-off of Short-Channel DG MOSFETs with High-*k* Gate Stack", *International Conference on Nanoscience & Nanotechnology* ***(ICNN-2013)***, 18th-20th November, 2013 held at Babasaheb Bhimrao Ambedkar University, Lucknow, U.P., India.

19. Gopal Rawat, **Sanjay Kumar**, Ekta Goel, Mirgender Kumar, Sarvesh Dubey and S. Jit, "An Analytical Study of Gaussian Doped Strained-Si on SOI MOSFETs for Optimizing *Off*-State Current", *International Conference on Nanoscience & Nanotechnology* ***(ICNN-2013)***during 18-20 November, 2013 at Babasaheb Bhimrao Ambedkar University, Lucknow, U.P., India.
20. **Sanjay Kumar**, Ekta Goel, Gopal Rawat, Mirgender Kumar, Sarvesh Dubey and S. Jit Jit, "Analytical Modeling of Subthreshold Swing Based on Surface Potential of Non-Uniformly Doped Double-Gate (DG) MOSFETs", *International Conference on Nanotechnology* ***(ICNT – 2013),*** 25th -26th October, 2013 held at HIT, Haldia, West Bengal.
21. Ekta Goel, Gopal Rawat, **Sanjay Kumar**, Mirgender Kumar, Sarvesh Dubey and S. Jit, "Surface Potential Based Subthreshold Current Model of High-*k* Gate Stack Double-Gate (DG) MOSFETs", *International Conference on Nanotechnology* ***(ICNT - 2013),***25th -26th October, 2013 held at HIT, Haldia, West Bengal.

List of National Conference (Oral/Poster) Presentations:

22. **Sanjay Kumar**, Mirgender Kumar, Sarvesh Dubey and S. Jit "Analytical modeling of Surface Potential and Threshold Voltage of Non-uniformly doped Double-Gate (DG) MOSFETs "*National Conference on Nanoscience and Instrumentation Technology (NCNIT-2013)* during 28th-29th March ,2013 held at NIT Kurukshetra.
23. Ekta Goel, **Sanjay Kumar**, Neetu Singh, Mirgender Kumar, and S. Jit, "Subthreshold Swing Model of Short-Channel High-k Gate Stack Double-Gate (DG) MOSFETs" *National conference on Research and Innovations in Electronics & Communication Engineering* ***(RIECE-2014)***, 10th-11th Oct, 2014 held at Noida Institute of Engineering and Technology, UP.