

# Dheeraj Kumar Sinha

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**AREAS OF INTEREST:** I/O Devices & Circuits, ESD Protection Circuits, Device-Circuit Interaction, VLSI System Design.

## ACADEMIC QUALIFICATIONS:

Degree	Year	Institution	CGPA/Percentage
Ph.D Electronics & Electrical Engineering VLSI (Microelectronics)	2012-2017	Indian Institute of Technology Guwahati	7.73/10
B.Tech Electronics and Communication Engineering	2006-2010	Rajiv Gandhi Technical University, Bhopal Madhya Pradesh	75.19/100

## PROFESSIONAL BACKGROUND:

Designation	Year	Organisation
Assistant Professor	July 2017 – till present	Indian Institute of Information Technology Bhagalpur
Research Associate	Feb 2017 – June 2017	Indian Institute of Technology Guwahati

## PROJECT UNDERGOING

- Funding Agency:** Start-up Research Grant (SRG), DST, GoI.  
**Designation:** Project Investigator  
**Duration:** 02 Years  
**Total Project Cost:** 24.92 Lacs
- Funding Agency:** Chip to Start-up (C2S), MeiTY, GoI.  
**Designation:** Co-Chief Investigator  
**Duration:** 05 Years  
**Total Project Cost:** 86.00 Lacs

## SELECTED PUBLICATIONS

- Dheeraj Kumar Sinha**, M. S. Ansari, Ashok Ray, Gaurav Trivedi, Amitabh Chatterjee and Ronald D. Schrimpf, “Fast Ionization-front Induced Anomalous Switching Behavior in Trigger Bipolar Transistors of Marx-bank Circuits Under Base-drive Conditions” IEEE Transactions on Plasma Science, Vol. 46, no. 6, pp. 2064-2071, June 2018.
- Dheeraj Kumar Sinha**, and Amitabh Chatterjee, “Spice Level Implementation of Physics of Filamentation in ESD Protection Devices” Microelectronics Reliability (Elsevier), Vol. 99, pp. 239-247, Dec 2017.
- Saurav Roy, Amitabh Chatterjee, **Dheeraj Kumar Sinha**, Rimma Pirogova and Srimanta Baishya, “2-D Analytical Modelling of Surface Potential and Threshold Voltage for Vertical Super-Thin Body Field Effect Transistor” IEEE Transactions on Electron Devices, Vol. 64, pp. 2106-2112, Apr 2017.
- Dheeraj Kumar Sinha**, Amitabh Chatterjee and Gaurav Trivedi, “Two Dimensional Numerical Simulator for Modeling NDC Region in SNDC Devices”, Journal of Physics: Conference Series, vol. 759(1), pp. 012099, Sept-2016.
- Dheeraj Kumar Sinha**, Amitabh Chatterjee and Ronald D. Schrimpf, “Modeling Erratic Behavior Due to High Current Filamentation in Bipolar Structures Under Dynamic Avalanche Conditions” IEEE Transactions on Electron Devices, Vol. 63, no. 8, pp. 3185-3192, Aug 2016.
- Dheeraj Kumar Sinha**, Vishnuram Abhinav, Amitabh Chatterjee, Gaurav Trivedi and Victor Koldyaev, “A Novel Capacitorless DRAM Cell Design Using Band-Gap Engineered Junctionless Double-Gate FET”, 29<sup>th</sup> IEEE International Conference on VLSI Design, Kolkata, Jan. 2016.
- Vishnuram Abhinav, **Dheeraj Kumar Sinha**, Amitabh Chatterjee and Forrest Brewer, “A Novel Co-design Methodology for Optimizing ESD Protection Device Using Layout Level Approach”, 29<sup>th</sup> IEEE International Conference on VLSI Design, Kolkata, Jan. 2016.
- Dheeraj Kumar Sinha**, Amitabh Chatterjee, Gaurav Trivedi and Victor Koldyaev, “Design of Band-gap Engineered Silicon-Germanium Junctionless Double-gate FET for ZRAM application”, 6<sup>th</sup> International Conference on Computers and Devices for Communication, Kolkata, Dec. 2015.
- Dheeraj Kumar Sinha**, Amitabh Chatterjee, Gaurav Trivedi and Victor Koldyaev, “Analysis and Design of ZRAM Cell for Low Voltage Operations”, 18<sup>th</sup> International Workshop on Physics of Semiconductor Devices, Bangalore, Dec. 2015.
- Vishnuram Abhinav, **Dheeraj Kumar Sinha**, Amitabh Chatterjee and Rajan Singh, “Methodology for optimizing ESD protection for high speed LVDS based I/Os”, 19<sup>th</sup> International Symposium on VLSI Design and Test, Ahmedabad, June, 2015.
- Ashok Ray, Gaurav Kumar, Sushanta Bordoloi, **Dheeraj Kumar Sinha**, Pratima Agarwal and Gaurav Trivedi, “FEM based Device Simulator for High Voltage Devices”, 21<sup>st</sup> International Symposium on VLSI Design and Test (VDAT), Roorkee, Apr-2017.

12. Saurav Roy, Shiva Puri Goswami, **Dheeraj Kumar Sinha**, Amitabh Chatterjee, and Victor Koldyaev, “Use of RTA in Super-thin Body Structures to Replace Critical Implants”, 18<sup>th</sup> International Workshop on Physics of Semiconductor Devices, Bangalore, Dec. 2015.

#### **TECHNICAL SKILLS:**

1. **Operating System:** Linux, MS windows.
2. **Tools:** TCAD Sentaurus, MATLAB, Mentor Graphics, Cadence Spectre, Cadence Virtuoso, HSPICE, Vivado, Modelsim.
3. **Hardware:** DSO, Function Generators, B1500A Semiconductor Device Analyser, Xilinx FPGA.

#### **OTHER TECHNICAL EXPERIENCE:**

1. Designed optimized Protection circuits without affecting the ESD robustness (Layout optimization) in 0.18 $\mu$ m bulk technology.
2. The impact of ESD parasitics on the CIS/CCD Image sensor performance was analysed based on simple lumped RC model of ESD protection devices using cadence (Virtuoso).
3. Worked with SPICE, process simulators (TSUPREM4, ISE-DIOS, 3-D TAURUS PROCESS), device simulators (MEDICI, ISE-DESSIS), Layout Editors (MAGIC and Cadence Virtuoso), Schematic Editors, Layout-vs.-Schematic tools.
4. Implemented AES algorithm and CODIC algorithm on Xilinx FPGA board.
5. Reviewer of research publications for in IEEE Transactions on Electron Devices, IEEE Transactions on Plasma Science, and IEEE Conferences, etc.

#### **TECHNICAL SOCIETY MEMBERSHIP:**

1. Member of IEEE Technical Society (From 01/01/2017 to Present)
2. Member of IEEE Electron Device Society (From 01/01/2017 to Present)
3. Student member of IEEE Technical Society (From 01/01/2013 to 31/12/2016)
4. Student Advisory Member of IEEE Student Branch, IIT GUWAHATI (From 01/01/2014 to 01/06/2017).

#### **TEACHING EXPERIENCE:**

1. **Courses Taken:**
  - **Undergraduate:** Basic Electronic Circuits, Digital Design, Analog Electronics, Semiconductor Devices & Circuits, VLSI Design, Analog IC Design, etc.,
  - **Postgraduate:** VLSI Signal Processing, SoC Design using Verilog, Design of ESD I/o Pads for High Speed RFICs.

#### **ADMINISTRATIVE POSITION AND ADDITIONAL RESPONSIBILITIES:**

1. Associate Dean, Student Welfare (Since July-2022)
2. Head of the Department, Electronics & Communication Engineering (May-2019 to July-2022)
3. Faculty Incharge, Civil Works (May-2019 to July-2022)
4. Faculty Incharge, Media & Spokesperson (Since July-2019)
5. Coordinator, Student Affairs (Oct-2018 to July-2022)
6. Faculty Incharge, Director Secretariat (Since July-2021)
7. Faculty Incharge, Store & Purchase (July-2020 to July-2022)
8. Faculty Incharge, GeM Buyer & Consignee (Since Sept-2020)
9. Warden, Boy's Hostel, IIIT Bhagalpur (July-2017 to Sept-2018)
10. Chairman, Anti-ragging committee (July-2017 to July-2022)

#### **EXTRA CURRICULAR ACTIVITIES:**

1. Organized workshop on “Introduction to MATLAB and its Applications” from 29/03/2019 and 30/03/2019 at IIIT Bhagalpur
2. Organized workshop on “Introduction to Robotics” from 08/03/2019 and 10/03/2019 at IIIT Bhagalpur
3. Organized Cultural program of IIIT Bhagalpur “SPANDAN-2K18”
4. Organized workshop on “Technical Training for Language Lab” from 13/10/2017 and 14/10/2017 at IIIT Bhagalpur.
5. Technical Volunteer in IEEE workshop in VLSI and MEMS Digital Design Flow 2014.
6. Technical Volunteer and Anchor in National Workshop GPU Programming and Application (GPA) organized by IIT Guwahati, IIT Bombay, CDAC Pune and NVIDIA.
7. Technical Volunteer in ADMAT-2015, 2016 organized by IIT Guwahati.
8. Student Volunteer in VDAT-2016 organized by IIT Guwahati.
9. Member of Event Manager in 49th Inter IIT Sports Meet – 2013.